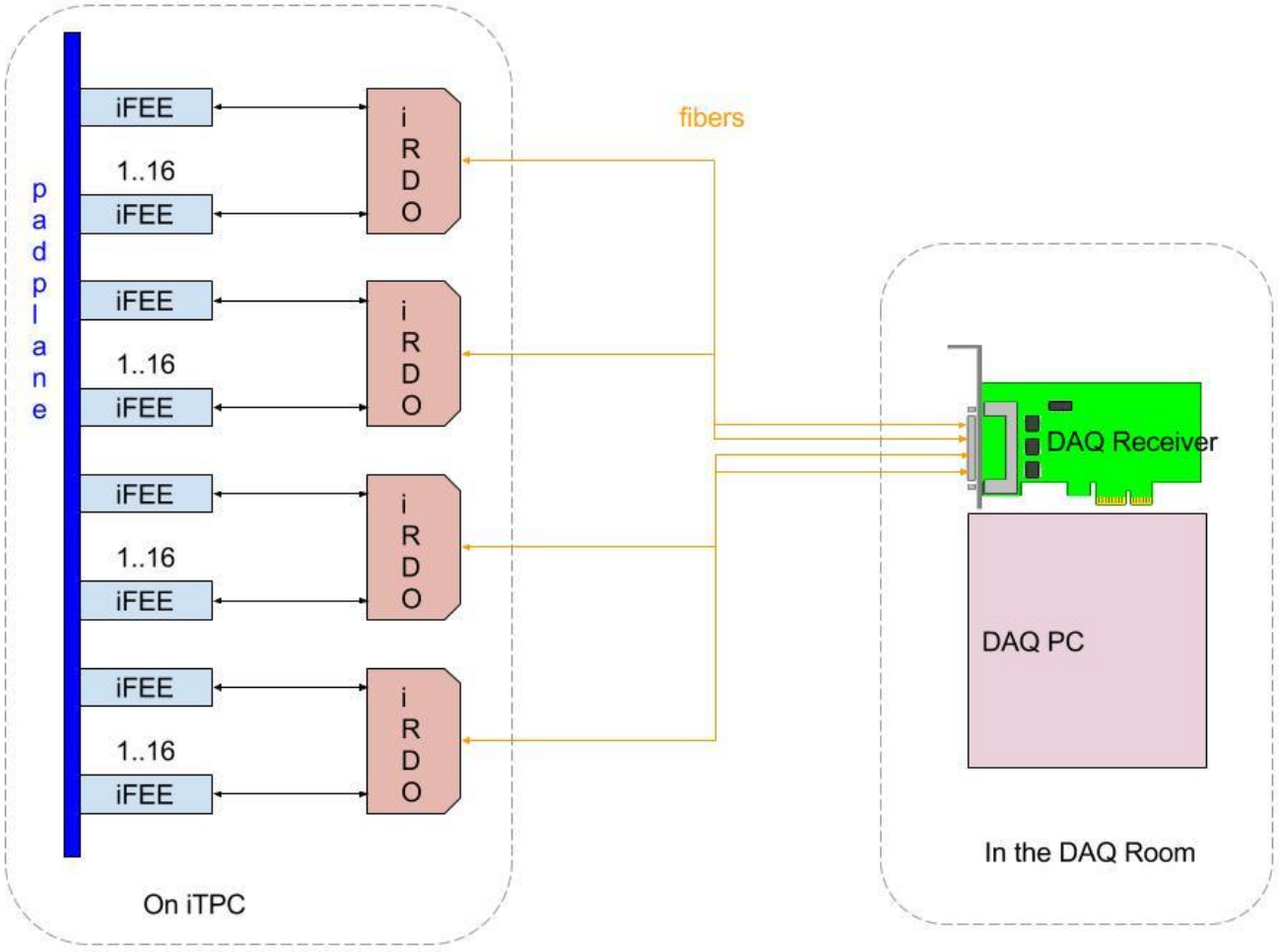
iTPC Electronics

T. Camarda, J. Hammond, T. Ljubicic,
B. Scheetz, A. Tkatchev, S. Valentino
(BNL)

Presentation Overview

1. iTPC Readout Scheme
2. Components
   a. Padplane (from the electronics perspective)
   b. iFEE (“Inner FrontEnd Electronics” card) & SAMPA ASIC
   c. iRDO (“Inner ReaDOut” card)
   d. DAQ Receiver Board (“RB”)
   e. DAQ Backend (PCs etc)
3. Testing & Installation
4. Resources Highlights
5. Cost Highlights
6. Schedule Highlights (with SAMPA details)
7. Risk Mitigation
8. Summary

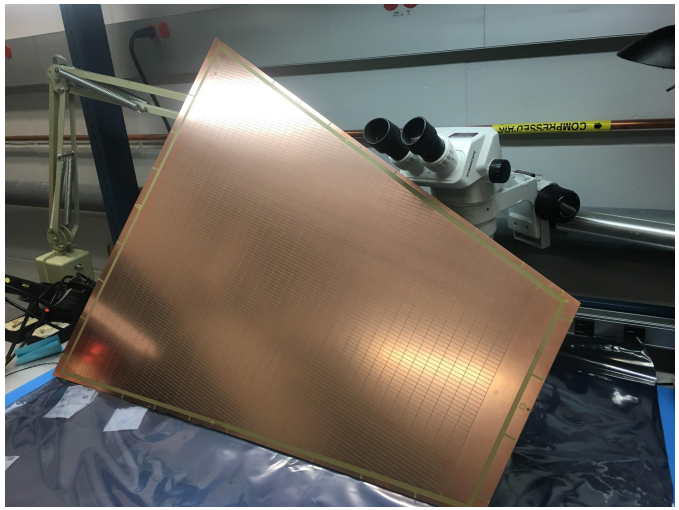
iTPC Readout Scheme (1 Sector shown)



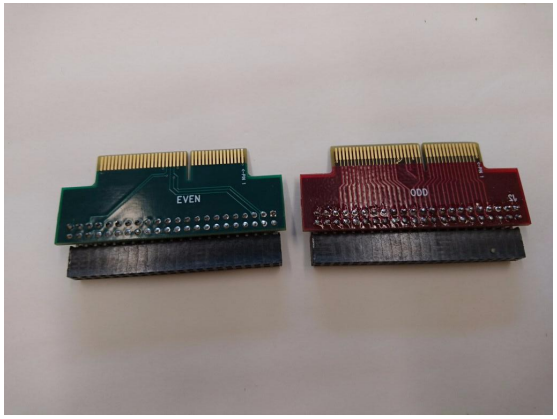
iTPC Readout Scheme (details)

- iFEE cards contain the preamplifiers & ADCs (“SAMPA” ASIC) and are plugged directly into the padplane
  - 64 channels (TPC pads) per iFEE (2 SAMPAs)
  - 55 iFEE cards/sector
- Each iFEE card sends data to an iRDO over short distance (2-3 ft) copper cables
  - Up to 16 iFEEs per iRDO
- iRDO houses the Trigger/Clock Interface, Power Supply Interface, Fiber Interface, PROM for FPGAs, storage memory and is control & multiplexer for the iFEE data
  - 4 iRDOs per sector
- iFEEs & iRDOs are mounted on the TPC wheel where water cooling exists reusing the exact same mounting structure as now
- Data from the iRDOs gets sent over ~50m fiber to “DAQ Receiver Boards” (RB) in “DAQ PCs” in the STAR “DAQ Room”
  - DAQ RB has 4 optical fibers ⇒ reads data from 4 iRDOs (= 1 TPC Sector)
  - 24 iTPC Sectors ⇔ 24 DAQ PCs each with 1 RB
- ⇒ similar to the current TPC in STAR

Padplane

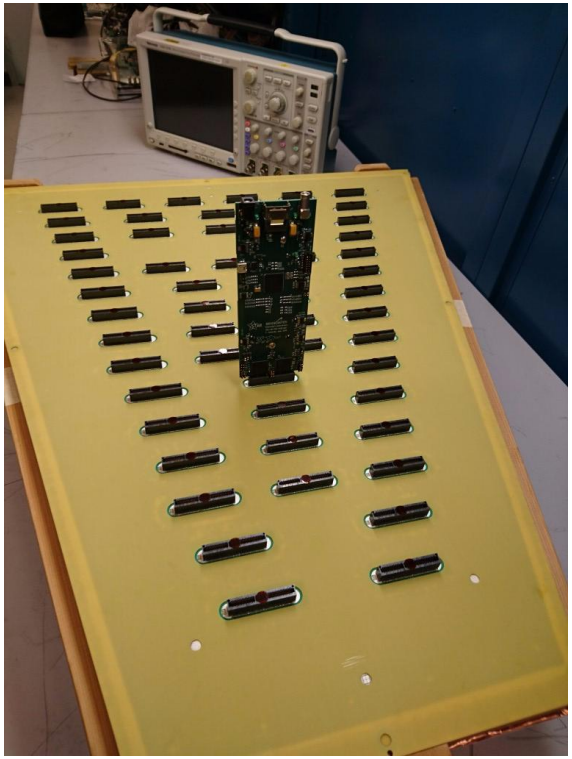


- 3440 pads (aka channels) total per padplane
- The longest trace length is 4.6” which is below the longest trace length of the current padrow (~5”)
  - Average trace length is only 1.8”
  - Intrinsic capacitive noise is expected to be comparable to the old system
- Higher density edge connectors (78 pins) for the iFEEs
  - 55 connectors per padplane
  - Each connector carries 64 signals, 8 grounds and 6 pins for a unique positional Id of the connector/iFEE
- We designed and produced adaptor cards which connect pads of 1 new row to 32 channels of our old FEE connector
  - 2 flavors: odd & even rows
  - Needed for testing of the new padplane with the old electronics
  - But also for Risk Mitigation (see later slides)



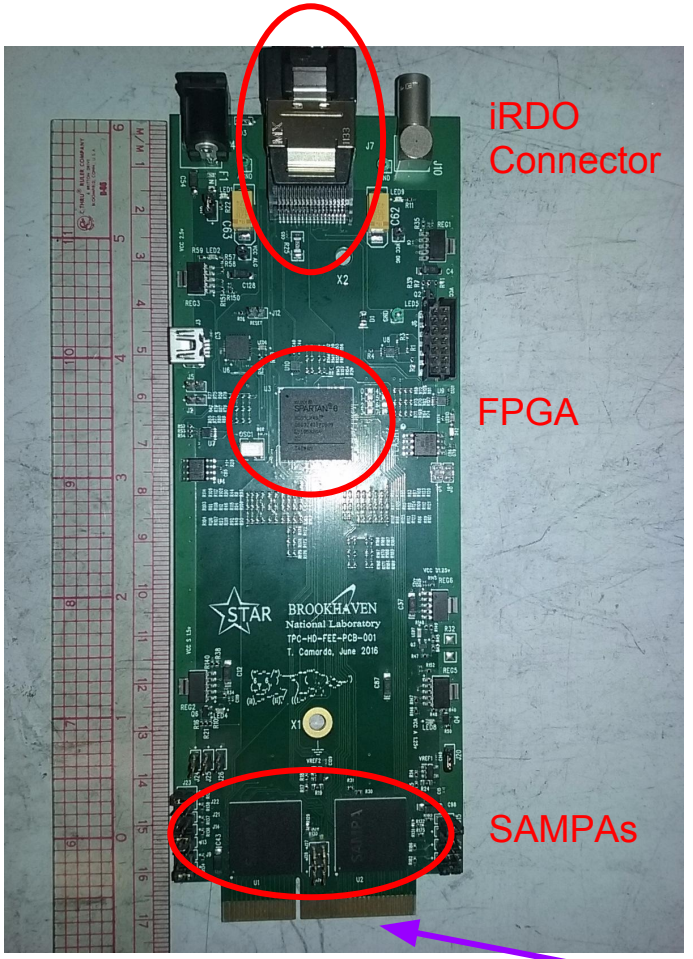
Padplane Testing

- In the next days we plan to verify & test the padplane
  - Connectivity tests for correctness (pad ⇔ connector pin)
    - Develop procedure for final Q&A
  - Noise tests with old and new electronics
    - Noise as a function of trace length



iFEE

- iRDO connector provides
  - Power to the iFEE
  - FPGA configuration
  - RHIC Clock & Trigger
  - Bi-directional serial data stream over copper
    - 10 Mb/s to the iFEE for control & pedestals
    - 640 Mb/s from the iFEE for data
- FPGA
  - Control of the iFEE & SAMPA
  - Mux for the serial SAMPA data (4 x 160 Mb/s) to the iRDO (640 Mb/s)
- SAMPA
  - Preamplifier, ADC, zero suppression, tail cancellation, signal shaping
  - Each SAMPA will use 2 serial lanes of 160 Mb/s each for data



SAMPA ASIC

- "SAMPA" is the main ASIC of the iTPC Upgrade
  - 32 channel preamplifier & shaper, 10 bit ADC, pedestal subtraction, zero suppression, tail suppression, digital filtering, serial readout; triggered & streaming mode
- Suitable for MWPC & GEM detectors (programmable gain, polarity & shaping time)
- Designed in Brasil for ALICE TPC & MCH Upgrade
- Combination of current ALICE/STAR ASICs PASA & ALTRO

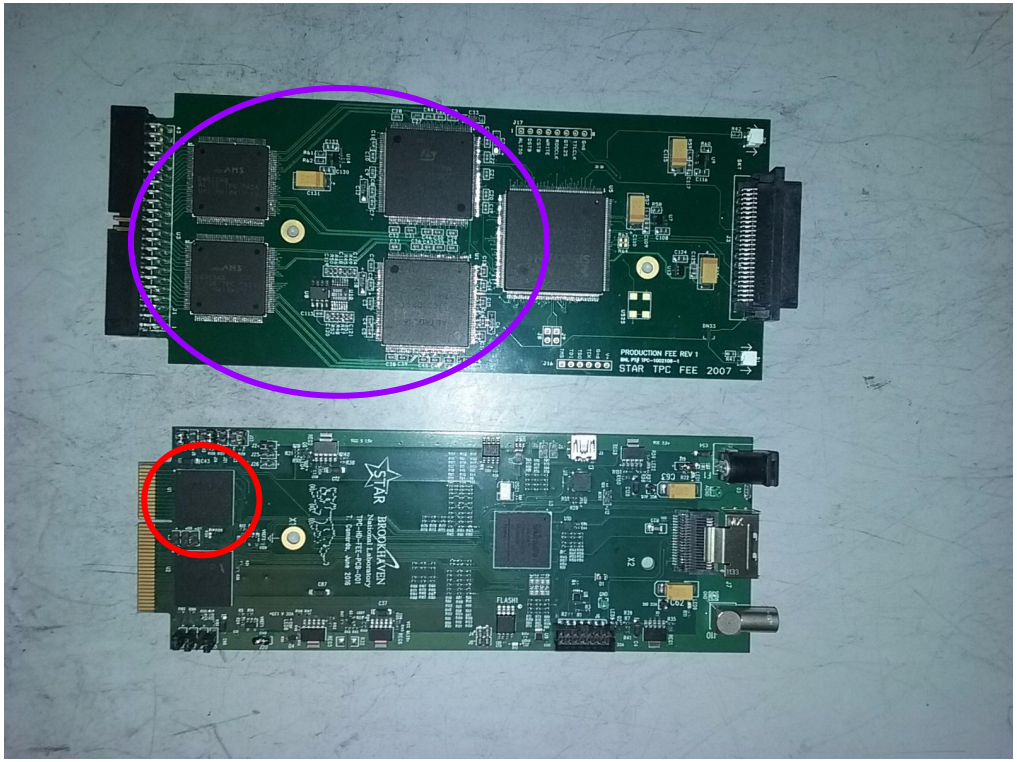
	SAMPA	**PASA+ALTRO**
Polarity	**Pos**/Neg	Pos (MWPC)
Shaping time	**160**/300 ns	190 ns
ADC	10 bits	10 bits
Noise	~950e at 40 pF	~same
Gain	4,**20**,30 mV/fC	13 mV/fC

SAMPA Evolution

- ASIC is still under design and will complete in Stages:
  - 1st Stage MWP1 (“Multi Wafer Prototype”) completed & tested
  - 2nd Stage (MWP2) completed & under test
    - First version with all of the functionality of 32 channels
    - Packaged in a BGA
    - Available to STAR and installed (see previous iFEE slides)
    - First tests all show good results but testing is continuing
      - Also at STAR
  - 3rd stage MWP3
    - Bug-fixes mostly
    - Other features?
  - Engineering Run
  - Final Run
- More on Schedule later...

SAMPA (comparison)

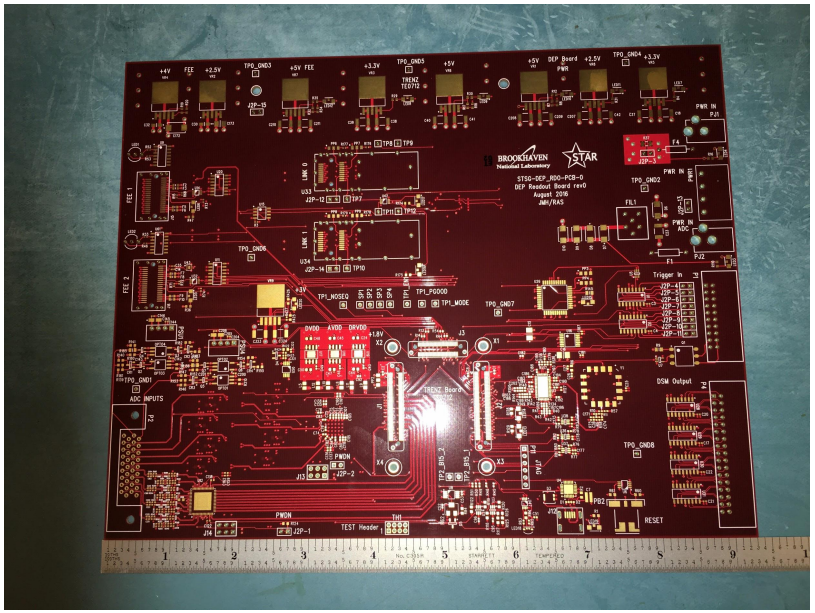
- Comparison to the current TPC electronics
  - 2 PASA chips & 2 ALTRO chips ⇒ 32 channels of preamp & ADC
  - 1 SAMPA chip ⇒ 32 channels of preamp & ADC



★ *Smaller*
★ *Denser*
★ *Simpler*
★ *Less power*
★ *Cheaper*

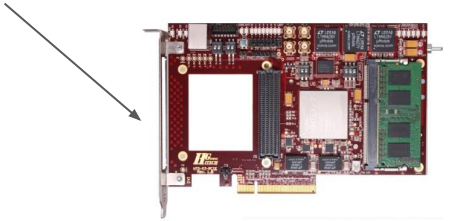
iRDO prototype

- A mixed prototype board for 2 different projects made since they have a lot in common
  - Same 2x fiber interface
  - Same Trigger/Clock interface
  - Same power supply
  - Similar footprint
  - Same FPGA module
- Reads out 2 iFEEs
- Expected at BNL tomorrow!
- Final iRDO version in design stage
  - Support for all 16 iFEEs
  - Final footprint & mounting scheme
  - non-iTPC functions to be removed



DAQ Receiver Board ("RB")

- The DAQ Receiver Board will be PCIe card which will accept data over fiber from 4 iRDOs (similar to now...)
- It will be housed in a commercial PC equipped with a standard motherboard
- A standard PCIe x4 V2 interface is enough for the necessary performance
- We haven't decided yet
  - Option A: develop our own generic Receiver Board based upon commercial FPGA modules
    - Cheaper, fully under our control, flexible, can be continuously developed & upgraded for other STAR future needs
      - But needs some (small) amount of engineering for the passive carrier card
  - Option B: purchase a commercial PCIe card with at least 4 fiber inputs
    - More expensive, no flexibility
      - no electrical engineering necessary although it will still need significant firmware development
- We have a candidate in house for Option B (HiTech)
- … but we are also moving on with the design of Option A for other STAR programs
- **⇒ Decision in mid-2017**



DAQ Backend

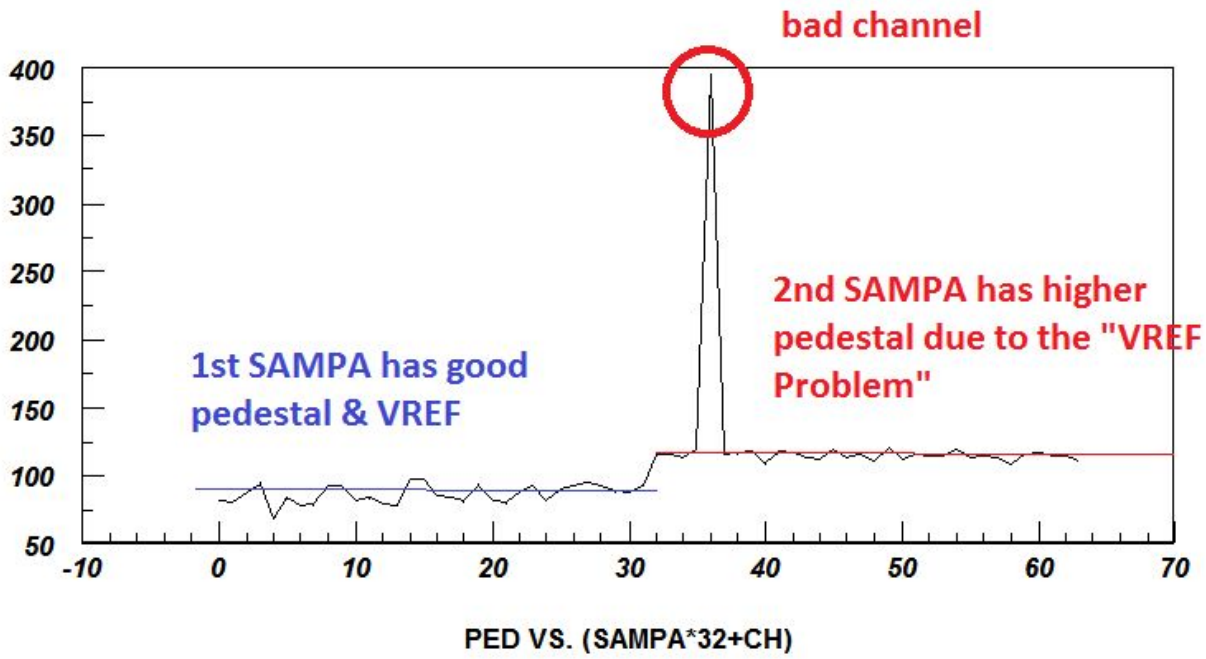
- Data is shipped from the iRDOs over ~50m fiber to the DAQ PCs in the “DAQ Room” of STAR
  - Away from radiation, accessible all the time
  - Same scheme as now…
- Each DAQ PC houses 1 Receiver Board which accepts data from 1 iTPC Inner Sector (total of 4 fibers per DAQ PC)
- Data is processed on the fly (same as now), clusters are calculated (same as now) & data is sent over Ethernet to STAR’s Event Builders (same as now)
- Each PC is a server-type 3U-high machine with
    - 1 PCIe x4 V2 slot
    - 8 GB of memory
    - 2 GbE ethernet spigots
    - 8 CPU cores @ ~1.6 GHz
    - No disk
    - Linux
  - ⇒ nothing special nor expensive… (same as now)
- Space & power for 24 such machines exists in the “STAR DAQ Room” racks

Testing (now - Jan 2017)

- Received an iFEE with SAMPAs late August ✔
- Testing of digital parts
  - USB standalone readout of the iFEE ✔
  - SAMPAs powerup and respond to control reads/writes as expected ✔
  - Clocking to SAMPAs good ✔
  - Serial data readout from SAMPAs to iFEE FPGA ✔
- Standalone testing of analog parts (noise) ✔
  - Next slides...
- Testing with the old padplane & comparison to the old FEE ✔
  - Next slides...
- After this meeting
  - Verify the iRDO
  - Develop iFEE ⇔ iRDO readout
  - Develop iRDO ⇔ PCIe RB fiber readout (Xilinx Dev kit AC701)
  - Develop configuration protocols (SAMPA, iFEE, pedestals load etc)
  - Wait for 20 SAMPAs ⇒ mount them on 10 iFEEs for continued testing

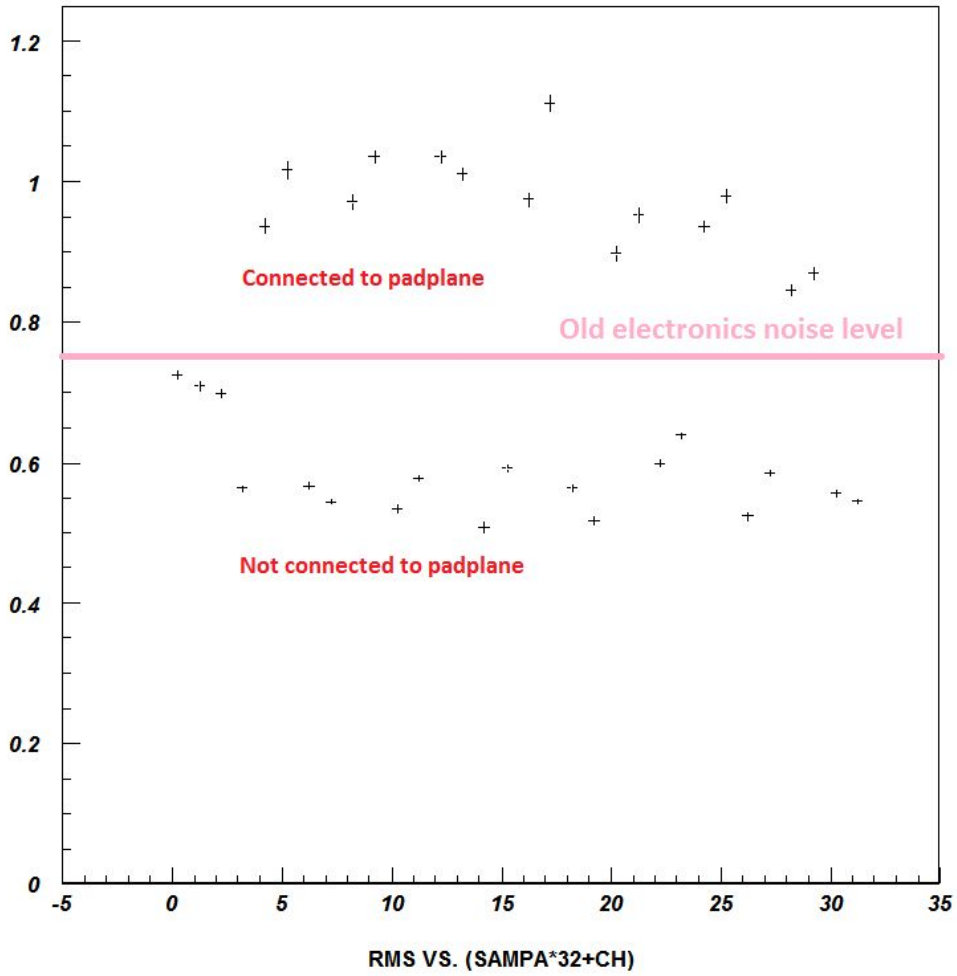
SAMPA tests with iFEE

- We obtained 2 *untested* SAMPAs
- 1 of them has the known/observed “VREF Problem” leading to subpar gain
  - Observed in 30% of the SAMPAs
  - Can be fixed
- 1 bad channel
  - Oh well...



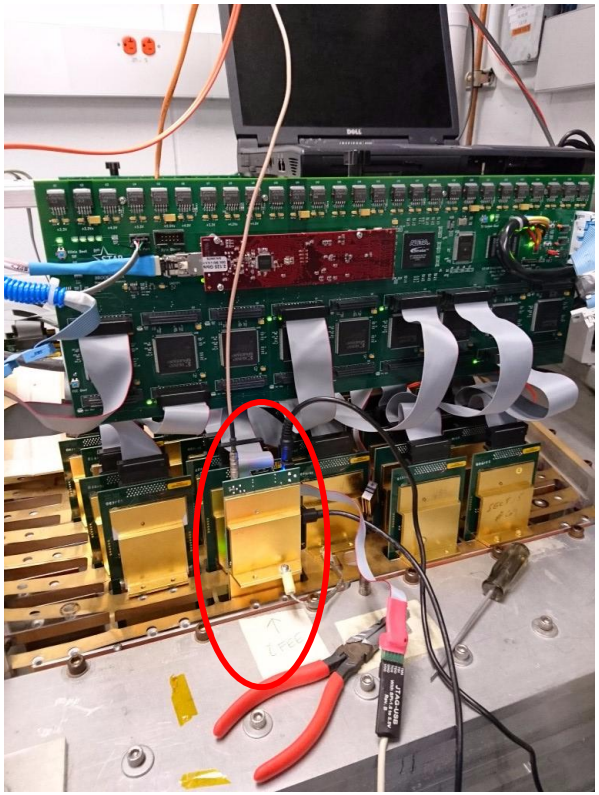
And more SAMPA tests…

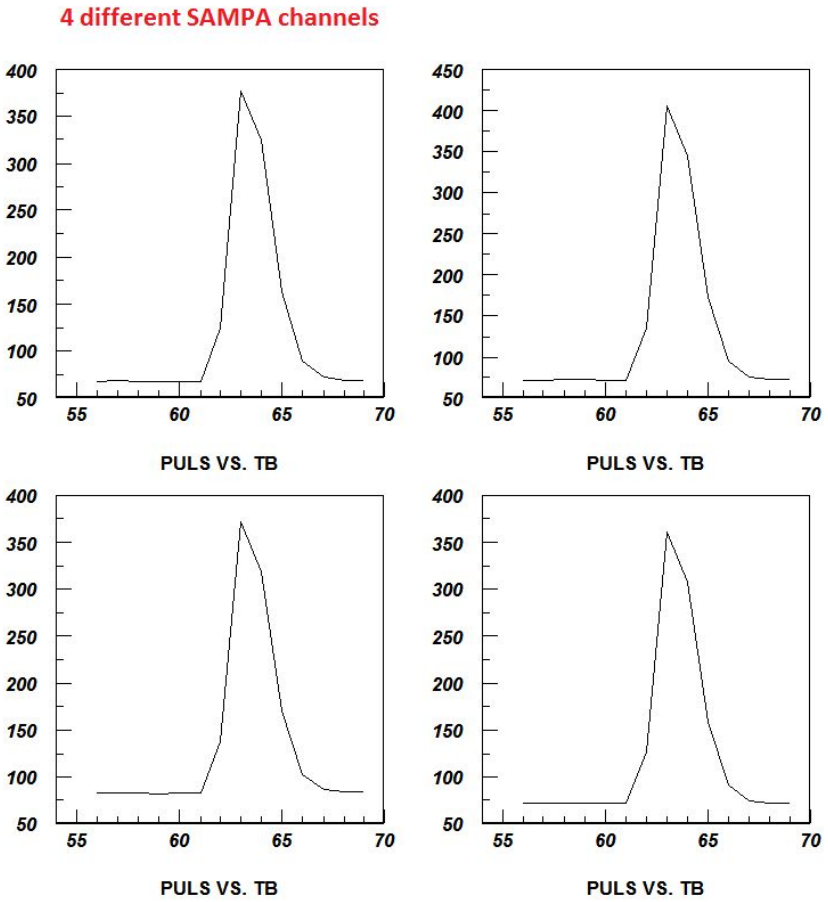
- Once connected to the padplane we observe larger noise on the connected vs unconnected pins
  - As expected (indeed required!) due to capacitance of the padplane traces (GOOD)
- iFEE has slightly larger noise than the old electronics
  - But it is still within our KPP requirements of <2 ADC ch (GOOD)
  - Also see next slide...



SAMPA tests continued

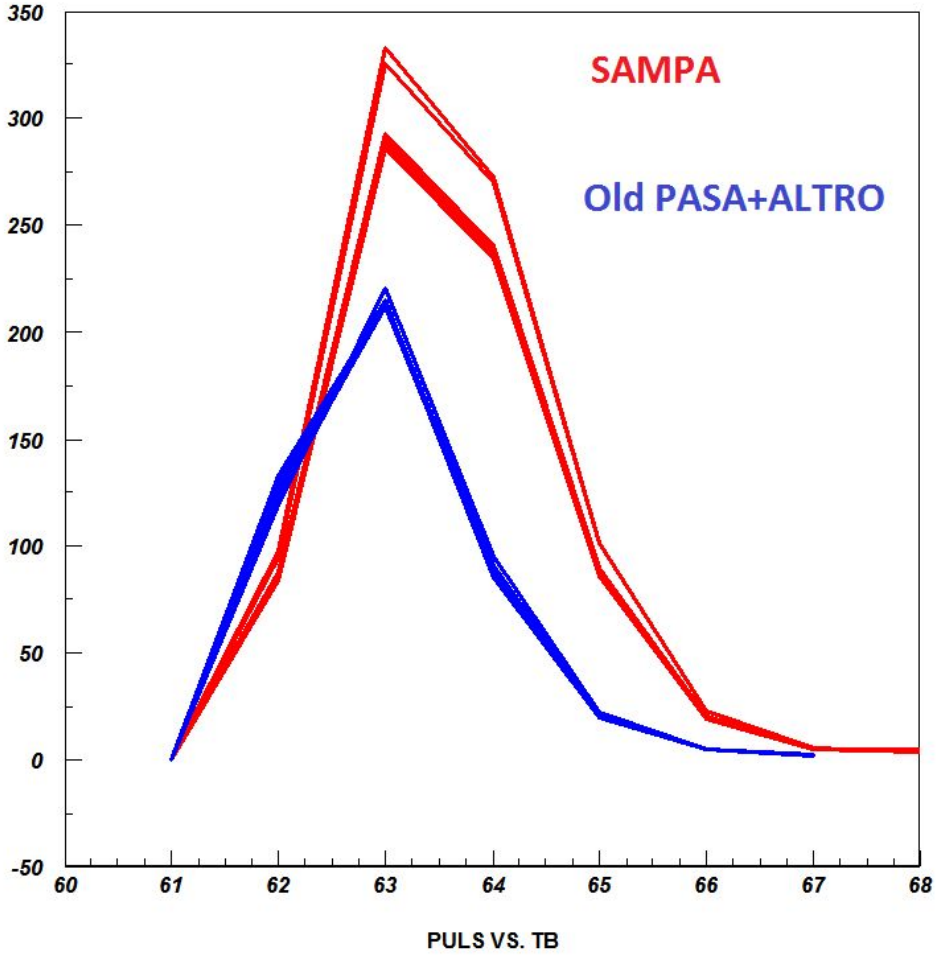
- Connected the new iFEE to our old padplane and pulsed the input via our usual TPC calibration pulser
- SAMPA response is good and uniform over all channels measured (GOOD)





Best SAMPA test

- Compared the SAMPA & the old electronics using the TPC padplane pulser in the exact same location
  - Same trace length (capacitance)
  - Same pulser shape
- The SAMPA gain was set at 20 mV/fC
  - The old PASA gain is ~13 mV/fC
- We observe the same ratio of the gain increase of the new electronics (GOOD)
  - The larger gain is also the cause of the larger observed noise by a similar factor ⇒ signal/noise same as now! (GREAT)
- Shaping time is also consistent with expectations (GREAT)



Testing (Jan-Jun 2017)

- We plan to test a readout chain in the actual STAR TPC using pp500 collisions
  - A most realistic test of the crucial parts of the chain: SAMPA, iFEE, iRDO
  - "Worst" beam conditions (and background) that RHIC can deliver
    - Far worse than BES-II
- Test Setup
  - 2 iFEEs ⇒ 1 iRDO prototype ⇒ 1 AC701 or HiTech PCIe fiber data receiver
- Test Goals
  - SAMPA response to actual physics TPC data
    - SAMPA community is very interested in this part
  - Electronics response to magnetic field
  - Electronics response to particle fluxes (SEUs and mitigation mechanisms)
  - Firmware testbed
    - Develop FPGA firmware as we go starting from basic readout, moving to required readout, ending in the fastest readout achievable
  - Software testbed
    - Develop the PC-side software (data unpackers & checkers etc)
- At the end of the period (May/June) we might also use the final version of our PCIe Receiver Board ("Option A" or "Option B")

Testing & Installation (2018)

- For the FY18 Physics run we plan to install 1 **full** iTPC sector and its electronics complement = 1/24th of the final iTPC
  - electronics installation by ~Dec 2017
- 55 iFEEs, 4 iRDOs, 1 RB, 1 DAQ PC
  - With required power supplies, fibers, etc
- **⇒ A full system test of all the final electronics components**

Human Resources Highlights

- 1 physicist
  - Subproject leader, architecture, electronics design, FPGA firmware
- 1 senior engineer
  - Electronics design, board schematics (padplane, iRDO, RB)
- 1 engineer
  - Board schematics (iRDO) and firmware support
- 1 junior engineer (actually a talented technician)
  - iFEE schematics, layout, component purchasing, manufacturing, test & installation
- 1 technician
  - Board layout, purchasing, manufacturing support, test & installation
- All above are part time only but we are in good shape for prototyping and concept testing!
- Production test & installation
  - For iFEE, iRDO & RB Q&A (2 months)
  - For deinstallation of the old electronics (1 month)
  - For installation of the new electronics (1 month)

Cost Highlights

	# items	# with spares	$ per item	$ all
SAMPA	2640	3500	$44	$154k
iFEE	1320	1580	$130 (wo SAMPA)	$206k
iRDO	96	116	$1300	$151k
DAQ Receiver	24	26	$3500	$91k
Cables, fibers, misc	-	-	-	$50k
Power Supplies	48	52	$600	$32k
DAQ PC	24	26	$3000	$80k
Totals				**$764k**

- No contingency, overhead, etc
  - Shown for relative comparison of the component costs only ⇒ see Flemming's talk for the full cost
- Still somewhat preliminary...
- Should have a much better estimate once all the prototypes have been tested in the actual TPC (Jan 2017)

Schedule Highlights

Sep-Dec 2016	iFEE, iRDO & Receiver Board firmware development Receiver Board (RB) design of Option A Final iRDO design
Jan-Jun 2017	Main system test of all components: iFEE, iRDO prototype, RB prototype Finish iRDO design & test Finish final iFEE design & test Finish RB design & test
Jul-Dec 2017	Final iFEE, iRDO & RB tested & evaluated Full Sector Test Electronics available (55 iFEEs, 4 iRDOs, 1 RB, 1 PC)
Jan-Jun 2018	Full Sector testing with padplane & in beam Preparation for full production & components purchasing
Jul-Oct 2018	Production of iFEE, iRDO & RB PCBs finished (but waiting for SAMPA?) All iRDOs & RBs tested DAQ PCs, fiber, power supplies installed & tested
Nov 2018	Mounting of SAMPAs to the iFEEs finished Installation of all components starts...

SAMPA Schedule Details

MWP3 Design Starts	now...
MWP3 BGA available	Jun 2017
Engineering Run Starts	Sep 2017
Engineering Samples Available	Feb 2018
Final Run Starts	Feb 2018
33% final SAMPA tested	Aug 2018
66% final SAMPA tested	Sep 2018
100% final SAMPA tested	Oct 2018

We could obtain SAMPAs at any (or all) steps marked in red. Even including the currently finished MWP2 run.

We don't yet know how this is going to unfold but we already started discussing possibilities of getting our required quantity from both the MPW3 Run and the Engineering Run.

Risk Mitigation

- Major risk is the SAMPA ASIC
  - It's a newly developed chip ⇒ many things could go wrong
    - But we plan to only use a subset of all its functionality (and not at the highest speed!) which we are already testing with MWP2
    - We are present at the weekly SAMPA Meetings and can point out any problems in advance and influence the design cycle *but we don't control the ASIC*
  - Schedule is the biggest risk
- Other risks are related to electronics performance (SAMPA analog behavior, noise, iFEE, iRDO, Receiver Board, achievable rates etc)
  - But we have extensive prototyping and testing throughout the whole time
    - Serious Jan 2017 tests in our real TPC with real data
    - Full Sector test in 2018 expected
    - Extensive Q&A of all components apart from the iFEE+SAMPA well in advance of installation

Risk Mitigation (cont'd)

- **If everything fails (SAMPA broken or delayed, other major electronics issues, etc) we have enough old/current electronics to readout every 2nd row of the new padplane**
  - We already prepared and tested adapters from new padplane → old electronics
    - This is BTW how we tested the noise vs trace length of the new padplane
  - We would have 20 new rows vs 13 old rows → slightly better than now
- … and the 2019 BES-II run will not be in jeopardy

Final Remarks

- iTPC Electronics Subproject is on a good track
  - First actual full SAMPA prototype looks good so far
  - iFEE with 2 SAMPAs looks good so far
  - Padplane looks good so far
- Major risk continues to be the SAMPA schedule
  - Although the current SAMPA schedule seems to hold
  - Some fear on our end regarding the formalities of SAMPA purchasing
- **The SAMPA chip is a very interesting ASIC for other detectors and for the future**
  - sPHENIX TPC expressed interest
  - EIC TPC?? Other EIC detectors??
  - Any other detector which isn't a trigger source and is GEM or MWPC based
    - STAR's Barrel ShowerMax Detector ("BSMD") needs electronics replacement
    - STAR's Forward Tracking detectors?